CLAIMS

1. A circuit for correlating an input signal comprising:

a parallel array of processing elements, each of said processing elements comprising an analog sampling circuit for sampling the input signal in response to a timing signal, and a circuit for scaling the resulting sample according to a predetermined scaling factor;

a timing circuit for causing said timing signal to be presented in time-delayed succession to successive ones of said processing elements; and,

means for summing the scaled output of said processing elements.

2. A circuit as in claim 1 wherein the scaling factors in successive processing elements correspond to the coefficients in a Fourier series approximation of a desired frequency response.

3. A circuit as in claim 1 wherein said timing circuit comprises a plurality of delay elements, the outputs of which are presented to successive ones of said processing elements.

4. A circuit as in claim 1 wherein said circuit for scaling comprises a multiplier having as inputs the output of said sampling circuit and a predetermined scaling factor, the outputs of said multipliers being summed.

5. A circuit as in claim 1 wherein the scaling factors in successive processing elements correspond to the coefficients in a Fourier series approximation of a desired frequency response, said timing circuit comprises a plurality of delay elements, the outputs of which are presented to successive ones of said processing elements, and said circuit for scaling comprises a

multiplier having as inputs the output of said sampling circuit and a predetermined scaling factor, the outputs of said multipliers being summed.

6. The method of correlating an input signal to an apparent reference signal, comprising:

generating a series of phase shifted analog samples of the input signal;

scaling successive ones of said samples by coefficient values representing the reference signal; and,

summing said scaled samples.

7. The method of claim 6 wherein said step of generating a series of phase shifted analog samples comprises providing phase shifted timing signals to a plurality of analog sample and hold circuits.

8. The method of claim 6 wherein said coefficient values comprise the coefficients of a Fourier series approximation of the frequency response of said reference signal.

9. The method of claim 8 wherein said step of generating a series of phase shifted analog samples comprises providing phase shifted timing signals to a plurality of analog sample and hold circuits.

10. A circuit for correlating an input signal with a desired frequency response, comprising:

a first and a second arrays of parallel processing elements, each of said processing elements comprising an analog sampling circuit for sampling the input signal in response to a timing signal, and a circuit for scaling the resulting sample according to a predetermined scaling factor;

a timing circuit for causing said timing signal to be presented in time-delayed succession to successive parallel pairs of said processing elements;

a summer for summing the scaled output of said processing elements comprising said first array; and,

a summer for summing the scaled output of said processing elements comprising said second array.

11. A circuit as in claim 10 wherein the scaling factors in successive processing elements of said first array correspond to the coefficients of a Fourier series approximation of the normal component of said desired frequency response and the scaling factors in successive processing elements of said second array correspond to the coefficients of a Fourier series approximation of the quadrature component of said desired frequency response.

12. A circuit as in claim 10 wherein said first array represents a normal channel and said second array represent a quadrature channel.

13. A circuit as in claim 10, 11 or 12 wherein said timing circuit comprises a plurality of delay elements, the outputs of which are presented to successive ones of said processing elements.

14. The method of correlating an input signal to an apparent reference signal, comprising:

generating a series of phase shifted analog samples of the input signal;

scaling successive ones of said samples by coefficient values representing the normal component of said reference signal;

scaling successive ones of said samples by coefficient values representing the quadrature component of said reference signal;

summing said normal scaled samples;

summing said quadrature scaled samples; and,

deriving the root mean square of said normal and quadrature sums.

15. The method of 14 wherein said step of generating a series of phase shifted analog samples comprises providing phase shifted timing signals to a plurality of analog sample and hold circuits.

16. The method of claim 14 wherein said coefficient values comprise the coefficients of a Fourier series approximation of the frequency response of said reference signal.

17. A circuit as in claim 1, 2, 3, 4 or 5 wherein said scaling factors are adjusted to alternate between scaling factors representing alternately a normal and a quadrature channel sets of coefficients of a Fourier series approximation of a desired frequency response.

18. A circuit for correlating an input signal comprising:

a parallel array of processing elements, each of said processing elements comprising a comparator for comparing said input signal with a predetermined reference value in response to a timing signal and outputting a value of +1 or -1;

a timing circuit for causing said timing signal to be presented in time-delayed succession to successive ones of said processing elements;

a multiplier for scaling the output of said comparator with a predetermined scaling factor representative of a normal or quadrature sine wave; and,

a summer for summing the scaled output of said processing elements.

19. A circuit as in claim 18 further comprising an averaging filter on the output of said comparator.

20. A circuit for correlating an input signal with an apparent reference signal wherein the apparent reference signal is embedded in an array of analog sampling circuits by means of scaling factors representative of the characteristics of said reference signal, and wherein the sampling point for the input signal advances through successive sampling circuits.